
Electrical I/O specification for Parallel Optics Module

- The following two slides are meant to help identify the options for the electrical I/O level definitions for the HIPPI-6400 parallel optics module. This is meant to define the expectations for both the optics module and protocol IC.
- Slide 2 is a compilation of typical PECL; IEEE's LVDS spec and a straw proposal from HP on an attempt to define optic module i/o levels which are a hybrid of PECL and LVDS.
- HP's goal is to define I/O which will allow the module to interface with both PECL and LVDS protocol modules.
- Slide 3 includes the information on the SuMAC chip from SGI for comparison.
- Action from 12/3 meeting:
 - Greg Chesson to verify information on the SuMac data.
 - Steve Joiner to compare with information obtained from SPIBOC.
 - All to provide input on values.

Proposed Hybrid PECL/LVDS I/O

	PECL	IEEE LVDS / Short	HP Proposal
Receiver			
Vin (diff. min.)	200mV	200mV	200mV
Vin (diff. max.)	2V	400mV	2V (AC) 400mV (DC, 1.2V bias)
Input Z (diff.)	100 ohms	90-110 ohms / 80-120 ohms	100 ohms
Transmitter			
Vout (diff. min.)	1200mV	250mV / 150mV	250mV
Vout (diff. max.)	2V	400mV / 250mV	400mV
Vol	AC coupled	925mV / 1025mV	1000mV
Voh	AC coupled	1475mV / 1375mV	1400mV
Vos (output offset)	AC coupled	1125-1275mV / 1150-1250mV	1.2V +/- 80mV
Output Z (diff.)	100 ohms	80-280 ohms	100 ohms
Absolute Limits			
Vi (input offset range)	AC coupled	0-2400mV / 825-1575mV	0-2400mV

HiPPI 6400 Proposed PECL/LVDS I/O

	PECL	SuMAC	HP Proposal
Receiver		Full / Reduce	
Vin (diff. min.)	200mV	150 mV / 80 mV	200mV
Vin (diff. max.)	2V	2.0 V	2V (AC) 400mV (DC, 1.2V bias)
Input Z (diff.)	100 ohms	?	100 ohms
Transmitter			
Vout (diff. min.)	1200mV	2120 mV / 800 mV	250mV
Vout (diff. max.)	2V	2410 mV / 1200 mV	400mV
Vol	AC coupled	276 mV / 700 mV	1000mV
Voh	AC coupled	2200mV / 1300 mV	1400mV
Vos (output offset)	AC coupled	NA / 1.0+/-0.1	1.2V +/- 80mV
Output Z (diff.)	100 ohms	? / ?	100 ohms
Absolute Limits			
Vi (input offset range)	AC coupled		0-2400mV